

AC/rd along a vertical direction from one position in a horizontal direction.

R E M A R K S

I. Introduction

In response to the pending Office Action, Applicants have amended Figs. 30-41 so as to include the legend "Prior Art". In addition, Applicants have cancelled claims 1-21, without prejudice, and have submitted new claims 22-40 in an effort to clearly distinguish the present invention over the cited prior art. With regard to the new claims, new claim 22 corresponds to original claim 1, new claims 28-33 correspond to original claims 8-13, respectively, new claims 34-38 correspond to original claims 16-20, respectively, and new claim 40 corresponds to original claim 21. New claims 23-27 and 39 are newly submitted. No new matter has been added.

For the reasons set forth below, it is respectfully submitted that claims 22-40 are patentable over the cited prior art.

II. The Rejection Of The Claims In View Of Karasawa

Originally filed claims 1-6 were rejected under 35 U.S.C. § 102 in view of USP No. 6,320,234 to Karasawa. Applicants respectfully submit that new claims 22-33, which have been presented in an effort to clarify the subject matter of the present invention, are not anticipated by Karasawa for the following reasons.

With regard to the newly submitted claim 22, one of the novel features of the invention is that the interconnection pattern which is disposed between the N-channel transistor and the P-channel transistor, and which is formed in the upper most interconnect layer of the CMOS cell, is electrically isolated. For example, as shown as element 9 in Fig. 1D of the specification, the upper most interconnect layer is not coupled to the N-channel transistor or the P-channel transistor. As a result, even there are changes in logic and/or interconnects occurring during the fabrication of the gate array semiconductor integrated circuit, by the arrangement of the plurality of CMOS basic cells having the foregoing interconnect pattern, the interconnect pattern can be utilized and therefore the effect of having only one layer of interconnect layer as an adjusting layer can be achieved.

Turning to the cited reference, Karasawa discloses an interconnect pattern in the upper most layer is electrically connected with the underlying transistors. As shown in Fig. 1 of Karasawa, interconnect 80 is coupled to the transistor 16. As such, Karasawa fails to disclose an interconnection pattern which is disposed between the N-channel transistor and the P-channel transistor, and which is formed in the upper most interconnect layer of the CMOS cell, which is not electrically isolated.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218

USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Karasawa does not anticipate any of new claims 22-33.

III. The Rejection Of The Claims In View Of Lee

Originally filed claims 14-20 were rejected under 35 U.S.C. § 102 in view of USP No. 5,874,754 to Lee. Applicants respectfully submit that new claims 34-40, which have been presented in an effort to clarify the subject matter of the present invention, are not anticipated by Lee for the following reasons.

With regard to new claims 34-40, one of the novel aspects of the invention as recited by these claims is that the first bend part provided at the upper portion of the gate of the transistor and the first bend part provided at the upper portion of the diffusion region of the transistor are bending in a mutually opposite direction, and the second bend part provided at the lower portion of the gate of the transistor and the second bend part provided at the lower portion of the diffusion region of the transistor are bending in a mutually opposite direction (see, for example, Fig. 27A of the specification). As a result, in the case where, for example, the first bend part of the gate of the transistor in one CMOS basic cell is to be connected to the first bend part of the diffusion region of the transistor in the neighboring CMOS basic cell using the foregoing design, the length of the interconnect can be advantageously shortened.

Turning to the cited reference, as shown in Fig. 2 thereof, Lee discloses the end

portion 20b of the gate region 20 and the end portions 30b, 32b of the source and drain regions 30, 32 are ending in the same direction (to the left), while another end portion 20c of the gate region 20 and another end portions 30c, 32c of the source and drain regions 30, 32 are bending in the same direction (to the right). Thus, at a minimum, Lee fails to disclose a first bend part provided at the upper portion of the gate of the transistor and a first bend part provided at the upper portion of the diffusion region of the transistor that are bending in mutually opposite directions.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Lee does not anticipate any of new claims 34-40.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

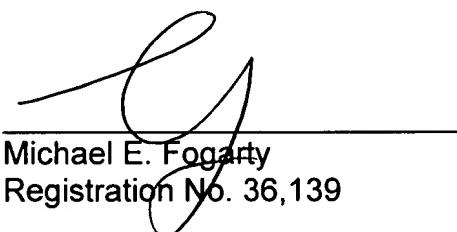
If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 7/1/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1-21, have been canceled without prejudice.

New claims 22-40 have been added as follows:

22. (New) A CMOS basic cell comprising:

an N-channel transistor and a P-channel transistor on a semiconductor substrate; and
an interconnect pattern which is electrically isolated and which exists between said N-channel transistor and said P-channel transistor,
wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell.

23. (New) The CMQS basic cell of Claim 1, wherein said interconnect pattern extending either along a perpendicular direction or along a horizontal direction relative to a boundary between said N-channel transistor and said P-channel transistor.

24. (New) The CMOS basic cell of Claims 22 or 23 further comprising: a power supply pattern, a master pattern and another interconnect pattern different from said

interconnect pattern,

wherein said another interconnect pattern exists between said N-channel transistor and said master pattern, said another interconnect pattern extending either along a perpendicular direction or along a horizontal direction relative to a boundary between said N-channel transistor and P-channel transistor, said another interconnect pattern electrically disconnected from said N-channel transistor and said P-channel transistor and formed in an uppermost interconnect layer.

25. (New) The CMOS basis cell of any one of Claims 22 to 24, wherein said interconnect pattern is mutually connected electrically with an interconnect pattern of another CMOS basic cell, when said CMOS basic cell is adjacent to said another CMOS basic cell.

26. (New) The gate array semiconductor integrated circuit of any one of Claims 22 to 25, wherein two or more said CMOS basic cells are electrically connected by a higher interconnect pattern located in a layer that is higher than said interconnect pattern.

27. (New) The gate array semiconductor integrated circuit according to Claim 26, wherein said higher interconnect pattern is located in a region between said

P-channel transistors and said N-channel transistors except the both ends of said interconnect pattern, and

wherein said interconnect pattern which intersects said higher interconnect pattern is electrically connected with a higher interconnect pattern except said higher interconnect pattern which intersects said interconnect pattern.

28. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to any one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a clock signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

29. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on

a semiconductor substrate; and

realizing a logic circuit including transistors connected to each other in parallel by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

30. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a composite logic circuit by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

31. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a control signal line by using said interconnect

patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

32. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit for a memory by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

33. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a flip-flop circuit having a scan test function by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

34. (New) A CMOS basic cell comprising:

an N-channel transistor and a P-channel transistor existing on a semiconductor substrate, said CMOS basic cell being electrical coupled with other adjacent CMOS basic cells;

wherein a gate of at least one of said N-channel transistor and said P-channel transistor has a hooked shape including a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof, and

a diffusion region of at least one of said N-channel transistor and said P-channel transistor having a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof,

said upper portion of said gate is bent oppositely to said upper portion of said diffusion region.

35. (New) The CMOS basic cell of Claim 34, wherein a first N-channel transistor and a first P-channel transistor are formed to extend along a vertical direction, and a second N-channel transistor is disposed on a side of said first N-channel transistor and a second P-channel transistor is disposed on a side of said first

P-channel transistor, and

a gate of each of said first and second N-channel transistors and said first and second P-channel transistors is formed in the hooked shape.

36. (New) The CMOS basic cell of Claim 35, wherein the gates of said first and second N-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when viewed along the vertical direction from one position in a horizontal direction, and

the gates of said first and second P-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second part of the other gate when viewed along the vertical direction from one position in the horizontal direction.

37. (New) The CMOS basic cell of Claim 35, wherein said first and second N-channel transistors share one diffusion region and said first and second P-channel transistors share one diffusion region,

each of said diffusion regions is divided into a shared diffusion region shared by said first and second N-channel or P-channel transistors and positioned between the gates of said first and second N-channel or P-channel transistors; a first dedicated diffusion region positioned on a side of said gate of said first N-channel or P-channel transistor opposite to said shared diffusion region; and a second dedicated diffusion

region positioned on a side of said gate of said second N-channel or P-channel transistor opposite to said shared diffusion region,

 said first bent part is formed in said first dedicated diffusion region, and
 said second bent part is formed in said second dedicated diffusion region.

38. (New) The CMOS basic cell according to any one of Claims 34 to 37, comprising, outside of a transistor region where said N-channel transistor are disposed, a fixed interconnect region where a power supply interconnect and a ground interconnect are disposed.

39. (New) The CMOS basic cell according to any one of Claims 34 to 37, said first bent part of said gate of said P-channel transistor and said first bent part of said diffusion region of said P-channel transistor of another CMOS basic cell is electrically connected with said higher interconnect pattern,

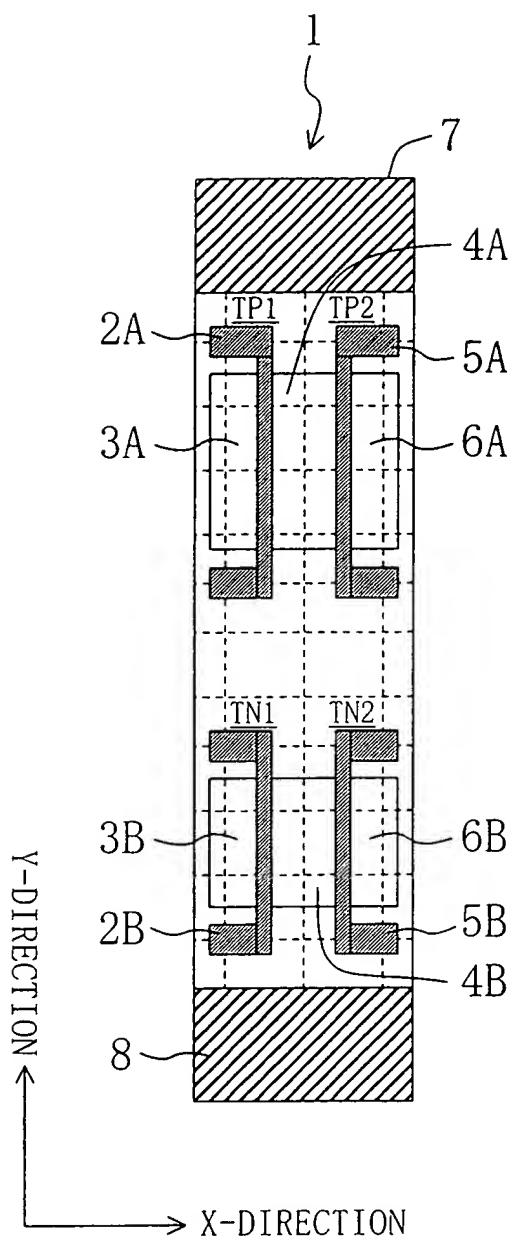
 wherein said higher interconnect pattern extends along a horizontal direction to the perpendicular from said N-channel transistor to said P-channel transistor.

40. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells arranged in a horizontal direction, comprising a step of arranging a plurality of CMOS basic cells according to any one of Claims 34 to 37 in the

horizontal direction in a manner that said first bent part of one CMOS basic cell overlaps said second bent part of another adjacent CMOS basic cell when viewed along a vertical direction from one position in a horizontal direction.

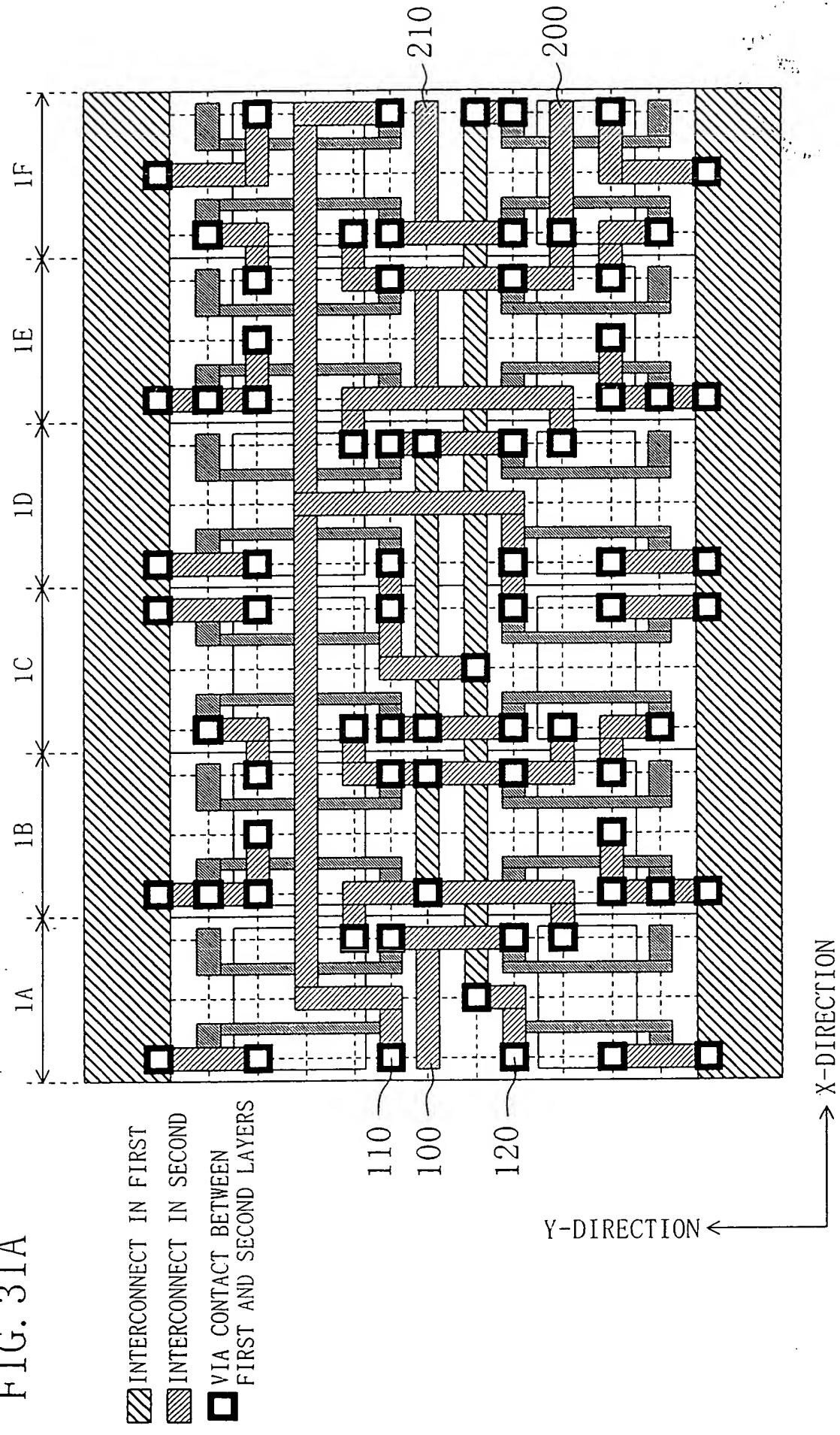
FIG. 30

PRIOR ART



PRIOR ART

FIG. 31A



Plot Art

FIG. 31B

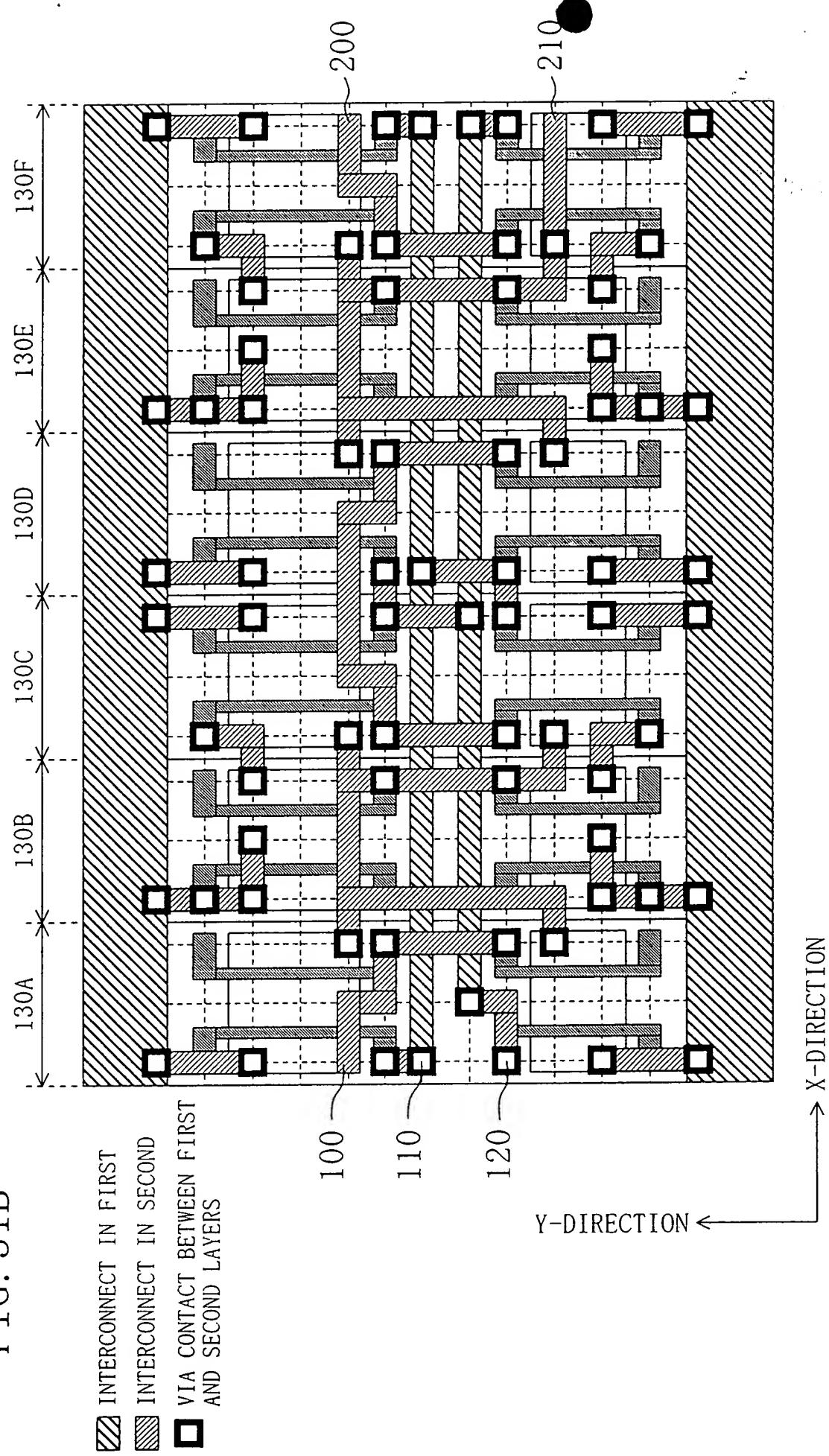
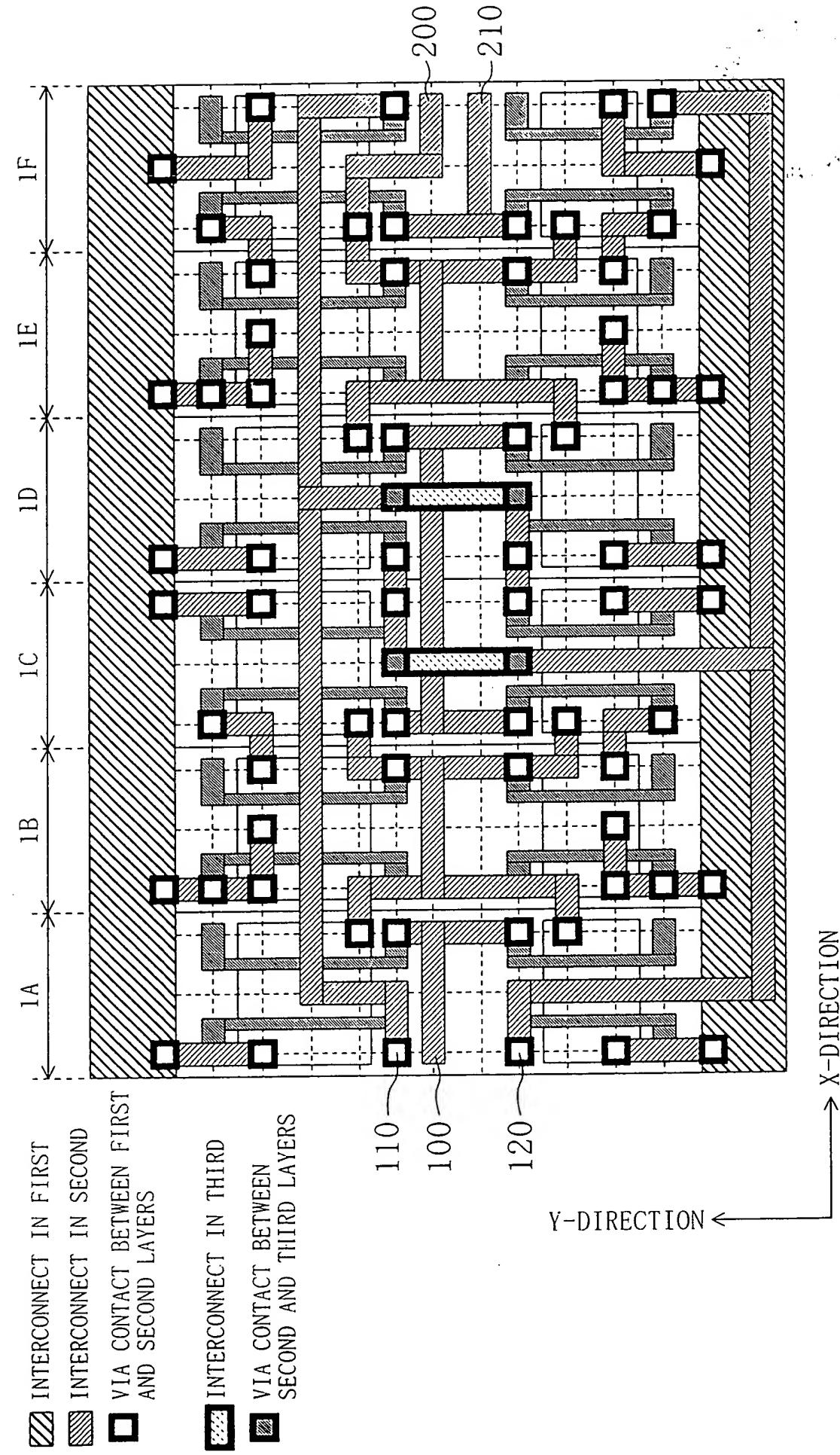


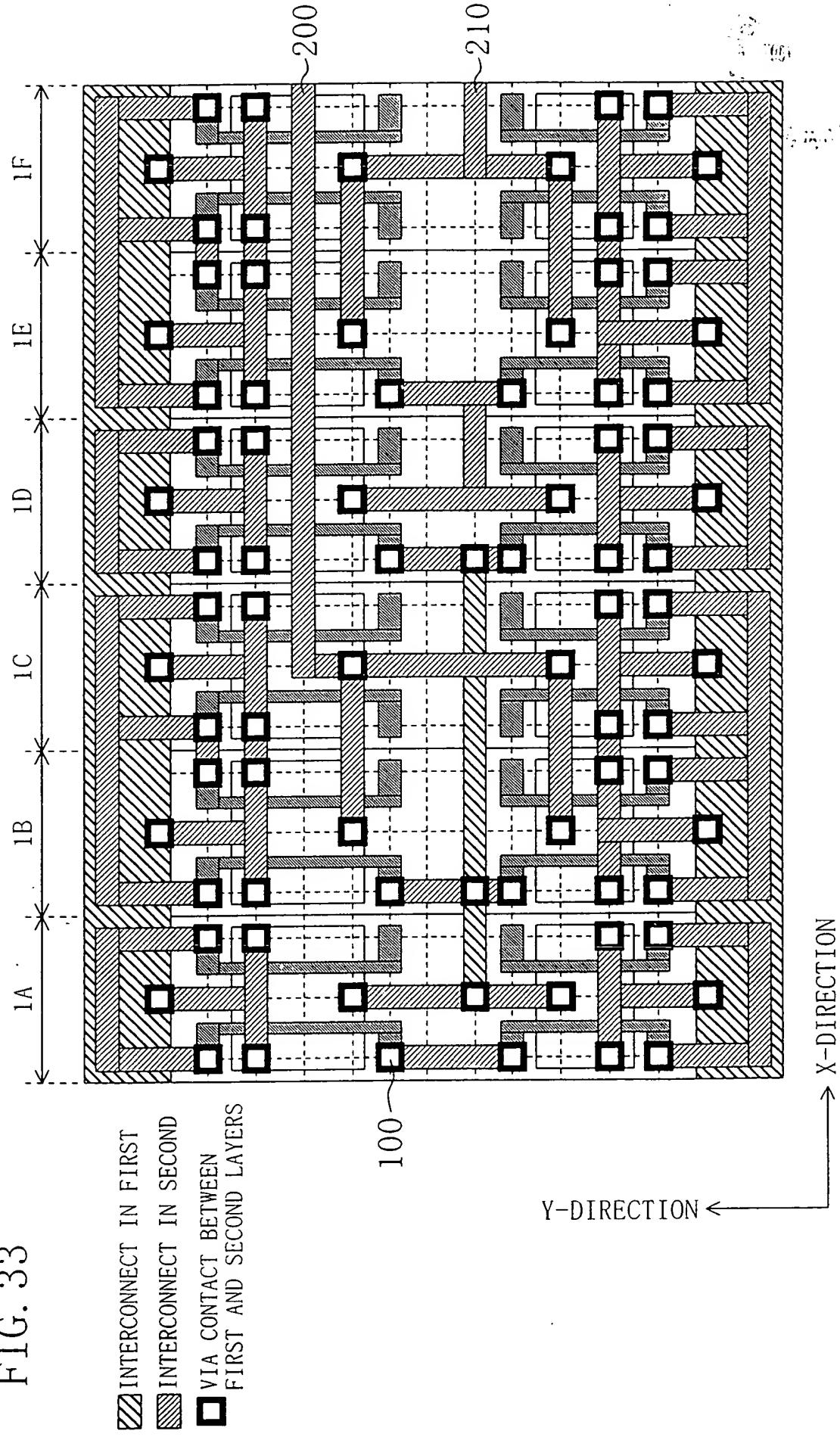
FIG. 32

Block A&T



Prior Art

FIG. 33



Risk Art

FIG. 34

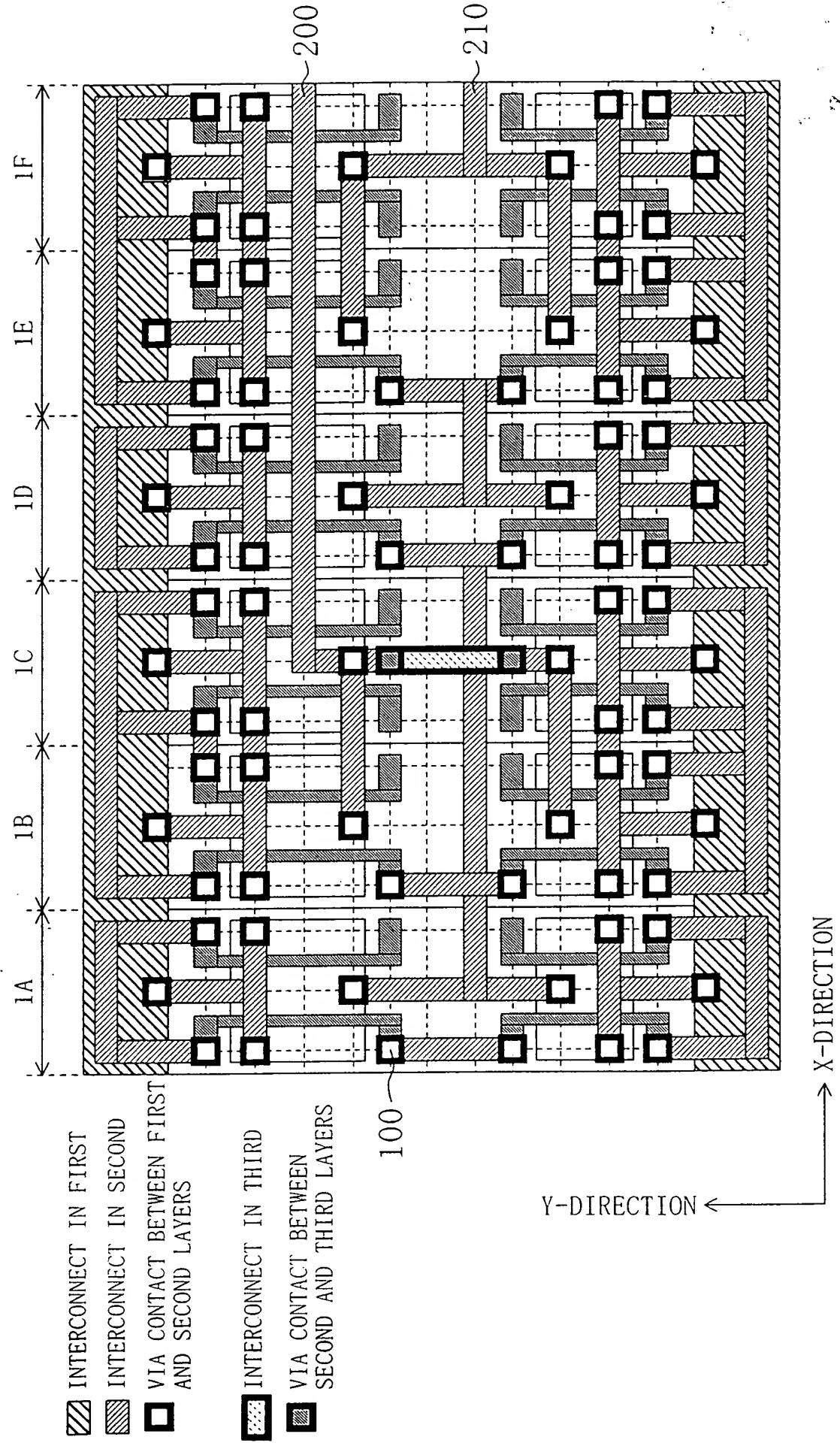


FIG. 35

PRIOR ART

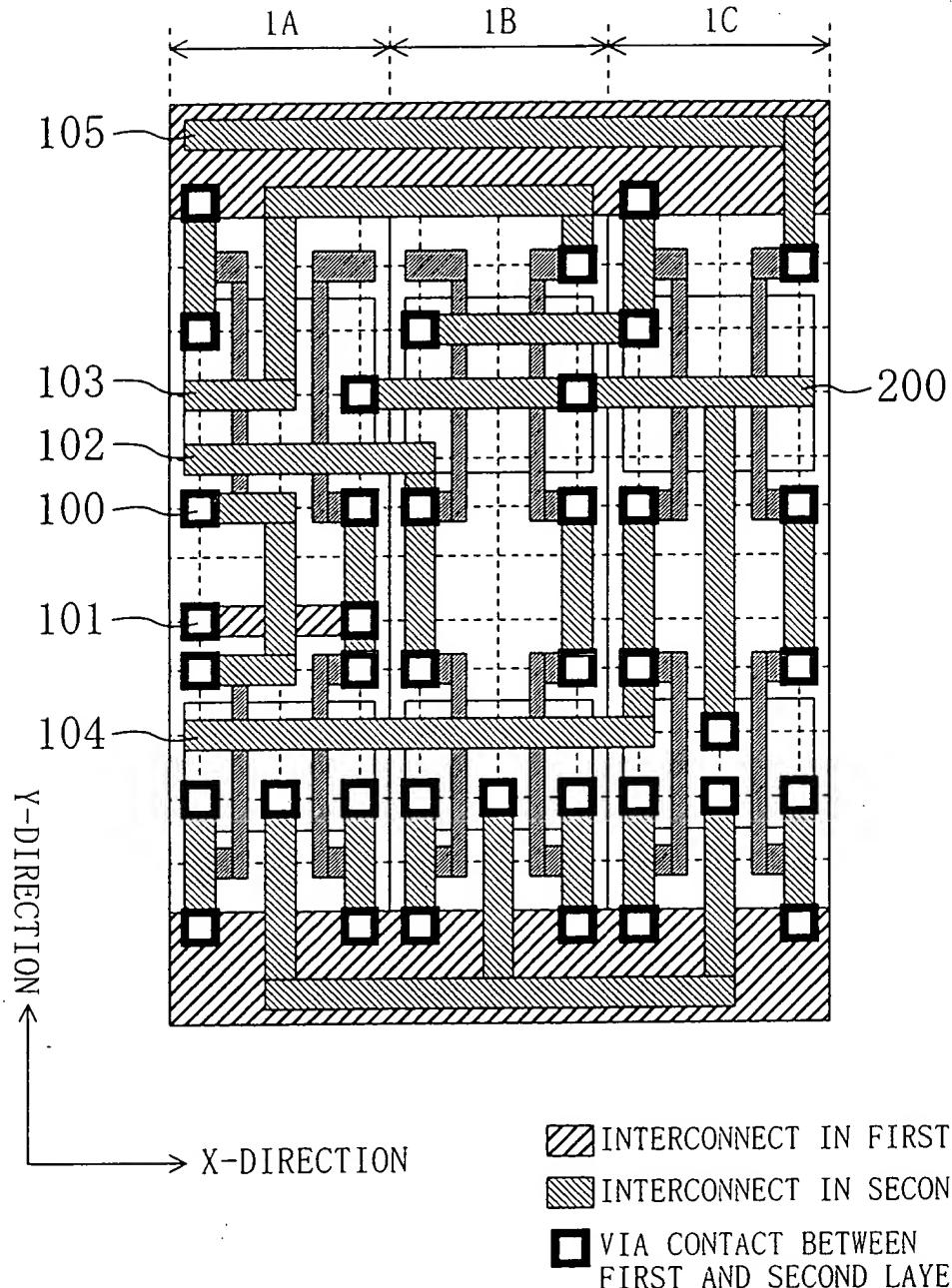


FIG. 36

PRIOR ART

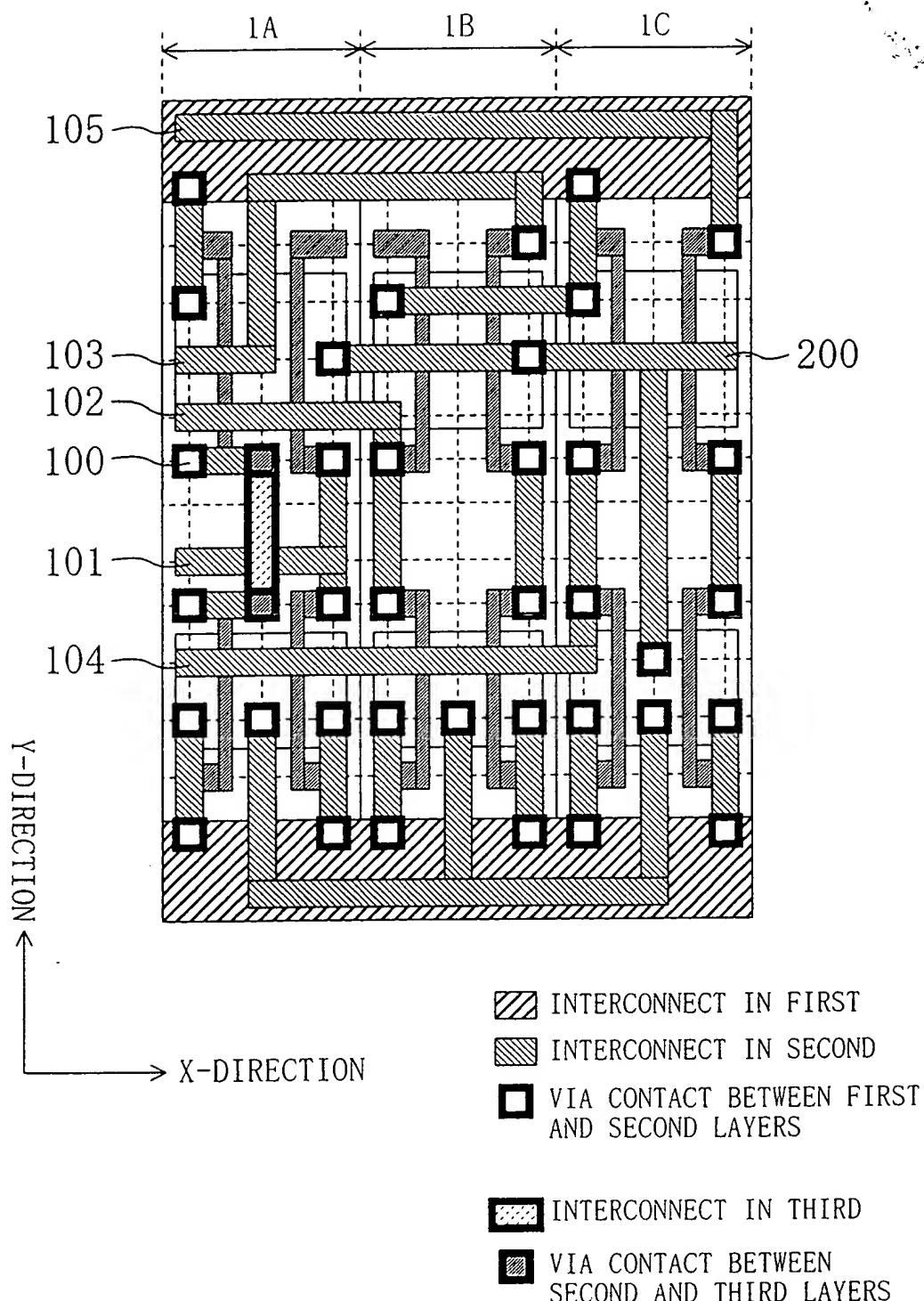


FIG. 37 PRIOR ART

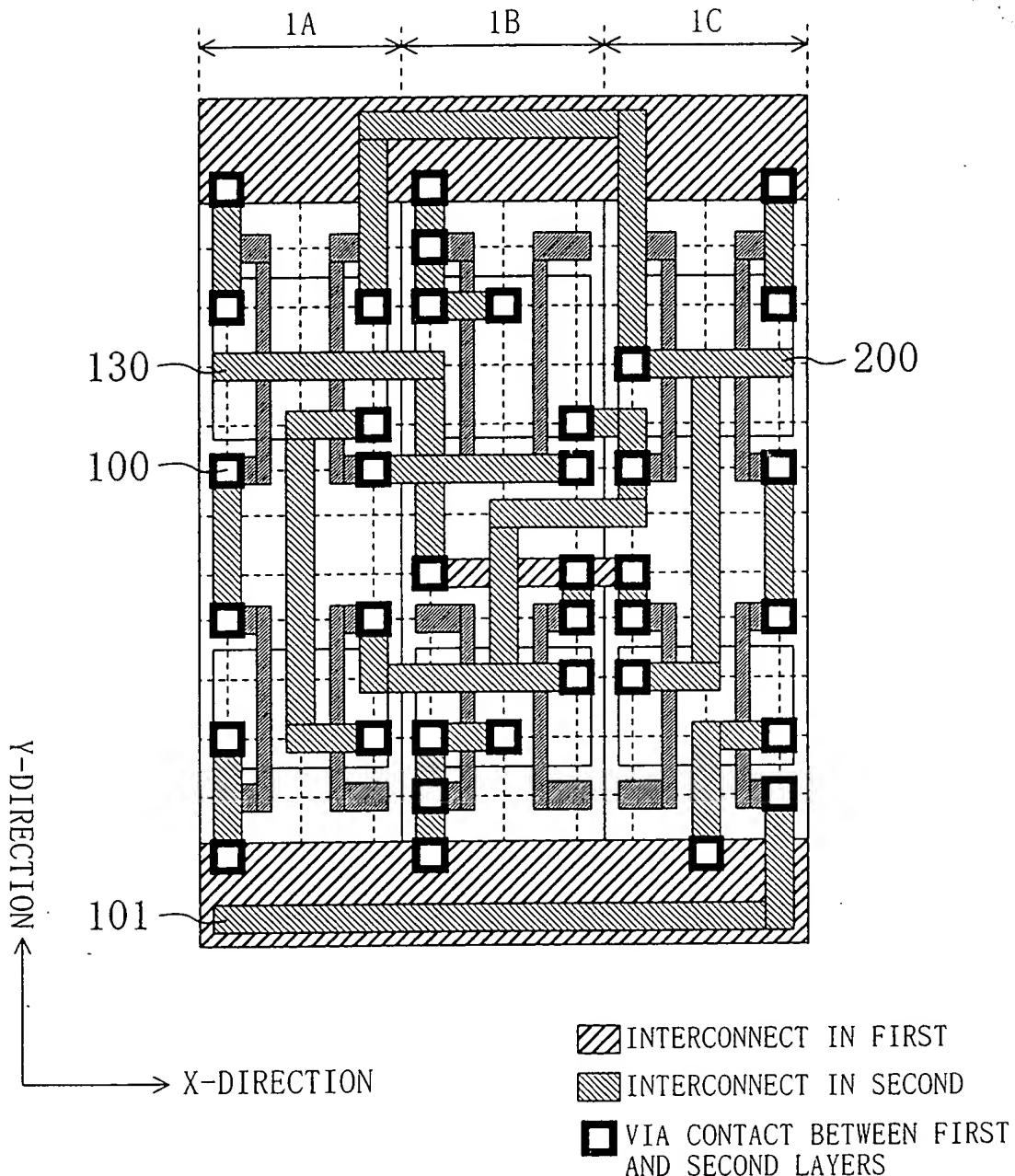


FIG. 38 PRIOR ART

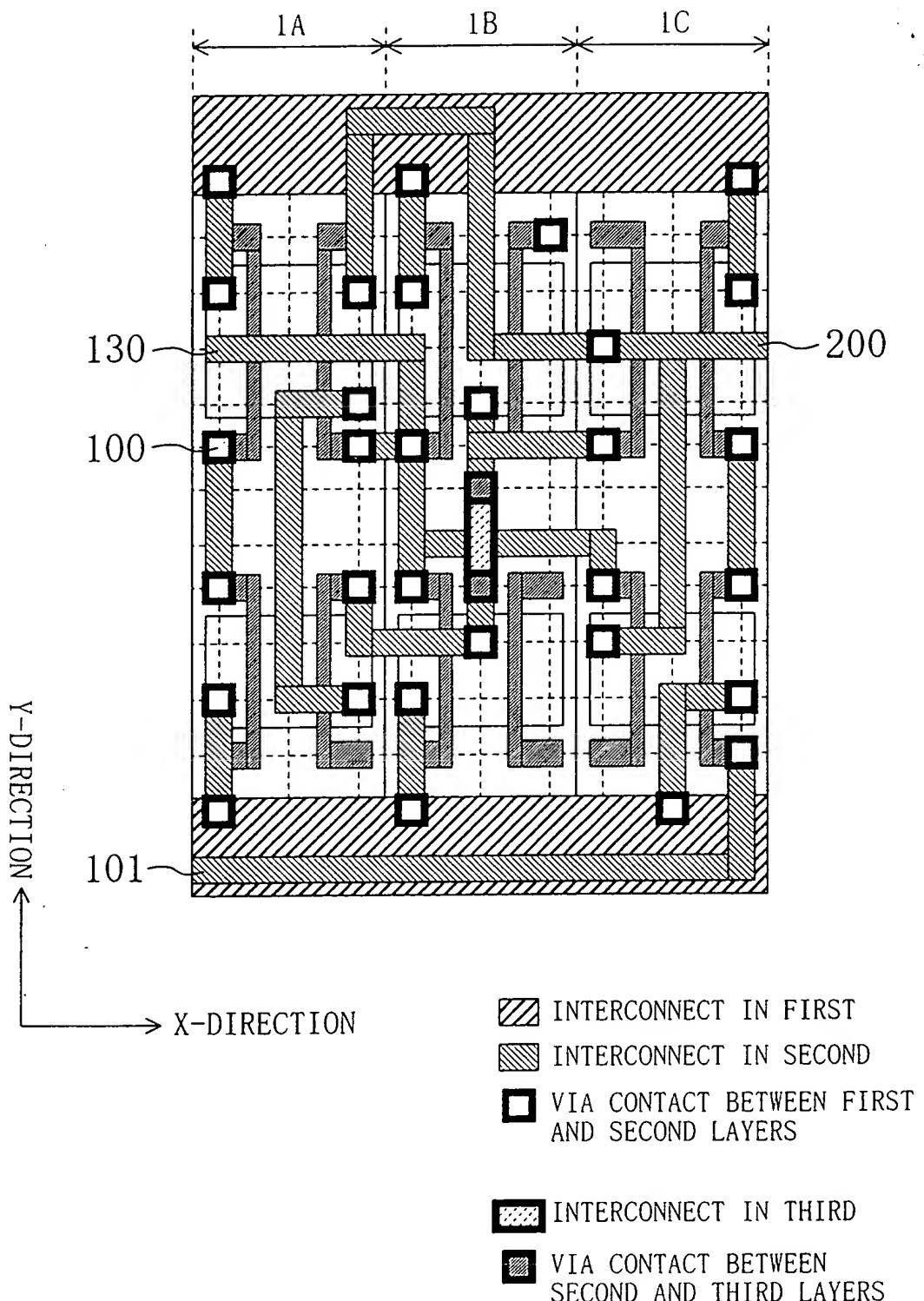


FIG. 39

PRIOR ART

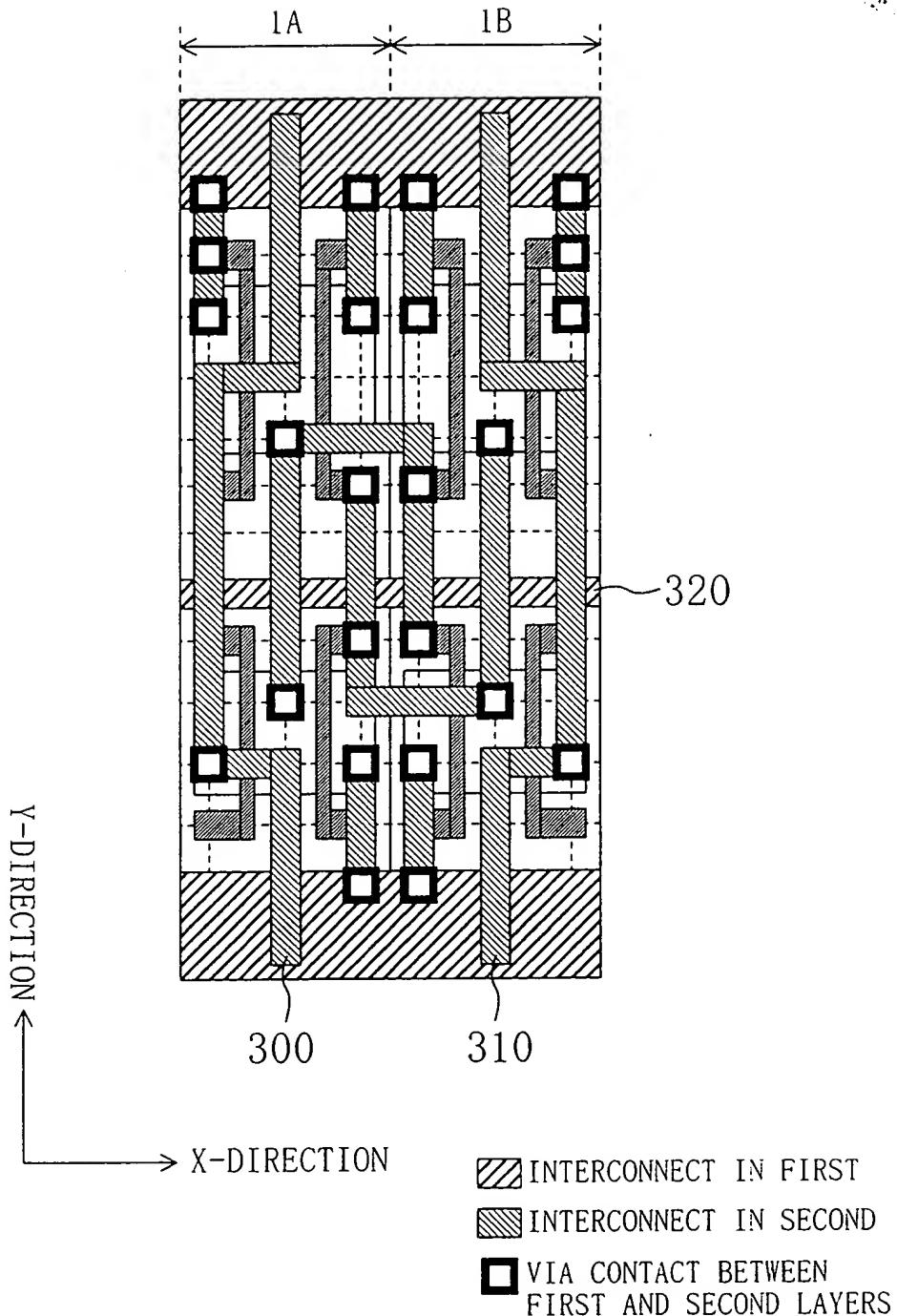


FIG. 40

PRIOR ART

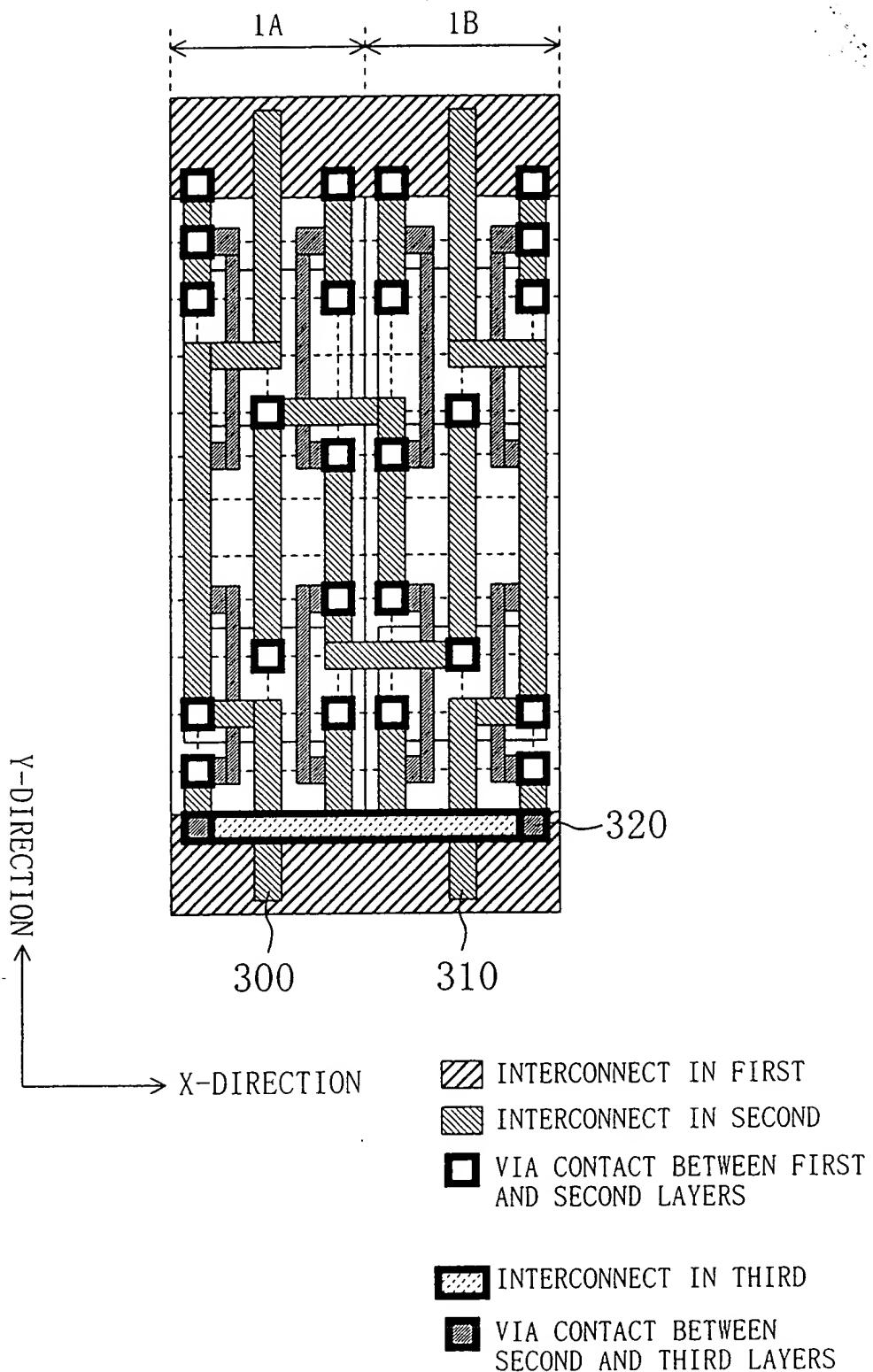


FIG. 41 Prior Art

